IN THE DRAWINGS:

Figure 17: replace reference "1750" with –1450--, replace "1460" with –1442--, and "1721" with –1460--.

Figure 20: replace duplicate reference labels 2010, 2012 and 2014 with 2002, 2004 and 2006 respectively, replace reference "1721" with –1460--.

Figure 25A: delete reference 2514

Figure 25B: delete reference 2528

Figure 26B: delete references 2629 and 2631

IN THE CLAIMS:

Please add new Claims 16-20, and amend Claims 1, 2, 4, 6, 9, 10, 14, and 15 as follows in this complete set of pending claims:

1. (amended) A digital system having a processor comprising a processor pipeline with a plurality of pipeline stages, a plurality of protected resources connected to receive data from certain ones of the plurality of pipeline stages and a pipeline protection mechanism, wherein the pipeline protection mechanism comprises:

a set of shadow registers;

interlock circuitry for anticipating access conflicts for each protected resource of the plurality of protected resources between the pipeline stages, an output of the interlock detection circuitry being controllably connected to the set of shadow registers; and

the set of shadow registers being interconnected with the processor pipeline such that a data item from a first pipeline stage can be redirected from a protected resource into a selected shadow register in response to an access conflict anticipated by the interlock circuitry so that a resource access conflict is resolved without stalling the processor pipeline.

2. (amended) The processing engine according to Claim 1, wherein the interlock circuitry comprises:

interlock detection circuitry operable to anticipate access conflicts for all of the protected resources and operable to form a stall vector signal indicative of anticipated access conflicts;

reservation and stall vector filtering circuitry connected to receive the stall vector signal and operable to select an available shadow register from the set of shadow registers in response to the stall vector signal; and

shadow management circuitry connected to the reservation and filtering circuitry, the shadow management circuitry having an output signal controllably connected to the set of shadow registers.

3. The processing engine according to Claim 1, wherein the interlock circuitry comprises arbitration circuitry for each protected resource such that each arbitration circuit is definable as a specific form of a single, generic arbitration function.

4. (amended) The processing engine according to Claim 1, including pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive the stall control signals output from the interlock circuitry based upon a result of arbitration between resources.

5. The processing engine according to Claim 1, wherein at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register.

6. (amended) The processing engine according to Claim 1, wherein the interlock circuitry comprises a stall vector filter, wherein the stall vector filter has a plurality of select filter stages connected in a serial manner such that each of the select filter stages is associated with a corresponding protected resource.

7. The processing engine according to Claim 1, wherein the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register.

8. The processing engine according to Claim 2, wherein the interlock circuitry further comprises arbitration circuitry for each protected resource such that each arbitration circuit is definable as a specific form of a single, generic arbitration function.

9. (amended) The processing engine according to Claim 8, wherein the reservation and stall vector filtering circuitry has a plurality of select filter stages connected in a serial manner such that each of the select filter stages is associated with a corresponding protected resource.

10. (amended) The processing engine according to Claim 9, further comprising pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive stall control signals output from the interlock circuitry based upon a result of arbitration between resources.

11. The processing engine according to Claim 10, wherein the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register.

12. The processing engine according to Claim 11, wherein at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register

13. The digital system of Claim 1 being a cellular telephone, further comprising:
an integrated keyboard connected to the processor via a keyboard adapter;
a display, connected to the processor via a display adapter;
radio frequency (RF) circuitry connected to the processor; and
an aerial connected to the RF circuitry.

14. (amended) A method of protecting a pipeline in a processor engine, wherein the processor includes a processor pipeline with a plurality of pipeline stages and a plurality of protected resources, the method comprising the steps of:

separately arbitrating, for respective protected resources, to anticipate access conflicts between the pipeline stages for each protected resource, and

redirecting a data item from a first pipeline stage from a protected resource into a shadow register in response to an anticipated access conflict so that a resource access conflict is resolved without stalling the processor pipeline.

15. (amended) The method of protecting a pipeline according to Claim 14, further comprising the step of selectively stalling stages of the pipeline depending upon the result of the arbitration for the respective resources to avoid resource access conflicts if the shadow register is not available to resolve an anticipated access conflict.

16. (new) The method of Claim 15, further comprising the step of selecting the shadow register from a plurality of shadow registers.

17. (new) The method of Claim 14, wherein the processor pipeline is updated periodically, and wherein the step of separately arbitrating is repeated for each protected resource prior to each periodic update of the processor pipeline.

18. (new) The method of Claim 17, wherein certain of the plurality of pipeline stages are subject to access conflicts, and wherein the step of separately arbitrating is performed in response to resource access signals provided by each pipeline stage that is subject to access conflicts, whereby additional control storage circuitry is not required for storing conflict control information.

19. (new) The processing engine according to Claim 1, wherein the processor pipeline is operable to update periodically, and wherein the interlock circuitry is operable to anticipate access conflicts for each protected resource during each pipeline period prior to each periodic update of the processor pipeline.

20. (new) The processing engine according to Claim 19, wherein certain of the plurality of pipeline stages are subject to access conflicts, and wherein the interlock circuitry is connected to receive resource access signals provided by each pipeline stage that is subject to access conflicts, whereby additional control storage circuitry is not required for storing conflict control information.